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Explicit Conditional Discharge P Flip Flop Design in Nanometer Range

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Abstract: On the present scenario clock misalignment and power consumption are the most critical design problems facing by the designers. In fabricated design, the clock system composed of timing structure block such as flip flops and latches. In any logic design, clock interconnection is the most power consuming mechanism. The total power is consumed by the clock system is around 20-40% of total chip power [1]. Another impact of technology advancement is the new design issues. Scaling tends to emphasize several other deficiencies like introducing parasitic capacitances, delay due to interconnection wires and synchronization with circuit design [2]. The proposed design of flip flop reduces the transistor count and furthermore achieves improved speed and power performance. This objective is met by designing S-edit software of Tanner Tool. The simulation process is performed using 1.8 V supply voltage at 90nm CMOS technology.

Key words: Power dissipation, Flip flop, clock cycle, conditional discharge.

Introduction:

A primary requirement for a digital circuit is perceptibly the performance of the function it is used to design for. When focusing on wholesome digital design, performance is more often expressed by the length of clock pulses or clock frequency. The smallest amount of the clock period is set by number of factors like the time it takes to propagate the signal during the logic, time to obtain data in and out, number of registers used and the improbability of the clock onset times [7]. In all digital designs, Flip-flops (FF) and Latches are the fundamental storage elements. They are accountable for exact timing, functionality and performance of the chip. These are the main cause of power consumption in synchronous circuits. The choice of Flip-flop design has a great effect to reduce power dissipation and high performance of the system. There are some factors which are desirable to designing of latches and flip-flops are:

1. High speed of the circuit or low propagation delay
2. Lustiness (robustness) and noise stability
3. To slow down power utilization
4. Used small chip area
5. Supply voltage competence for system
6. Low glitch
7. Insensitivity in clock edge
8. Less internal activity when input data is low
9. Uses of least numbers of transistors

The output of the combinational logic circuits is basically the function of present values of input so an adequate amount of time has elapsed for the logic condition to settle. Still, all useful systems require storage of state information. A standard memory element has as

internal memory and modest electronic equipment to manage the internal memory. For any sequential circuit, clock initiated to the memory element that reads data values and stores this. Probably after some hold-up time, the output values reflect at the output terminal.

Basically there are two approaches to structure a memory in CMOS digital circuits. The first approach uses positive or regenerative feedback. At this point, one or more output signals are purposely feedback to the input terminals to enhance the gain of the system. This brings a reference to multivibrator circuits. In the second approach, memory element is constructed in the circuit to store signal values for the upcoming output values. Furthermore this technique demands regular refreshing to the circuit as charge tends to leak away by means of time. This approach is tremendously admired in MOS world. There are several subclasses of Flip-flops [3, 5]. These classifications are predominantly based on the performance of input signal, number of transistor used, clock signal and the output of the flip-flop. The following table-1 is used to describe the type and working of the flip flops.

TABLE I

S. No	Type of Flip flop	Working
1	Master-Slave and Pulse Triggered	It is designed as a latch pair in series which works in different phases of clock pulses
2	Static Flip Flop	These flip-flops are a group of flip-flops that can preserve their stored value even if clock is stopped
3	Dynamic	The stored value will be destroyed in this flip flop but it can attain high speed and lesser power utilization
4	Multi-Clock Phase Flip-Flop	In master-slave flip-flops different clock phases are required. So, if master and slave latches have similar structures two clock phases are needed
5	Single Clock Phase Flip-Flop	The number of clock pulses is reduced to one by changing the structure of two Latches in master slave flip flop. True Single Phase Clock (TSPC) flip-flops can operates on high speed because of skew time
6	Single Edge Triggered	It can operate on the rising edge or the trailing edge of the clock pulses
7	Double Edge Triggered	They capture data on both edges of a clock pulse. The sampling of input is completed by both positive and negative edge of the clock
8	Single Ended	Only one input and output is required to frame this circuit
9	Differential Flip-Flop	These type of flip flops require equally true and complement inputs and generates both true as well as complementary output

I. Conventional Explicit Type P-FF Design

This flip flop contains a NAND based pulse generator and a semi active true single phase clock (TSPC) structure shown in Fig: 1. By the use of this technique, power utilization can be drastically reduced and increases the efficient energy. It is also named as Explicit DCO (data close to output). The deviation of pulse width to pulse distribution network, confines the circuit performance [9]. Due to transistor inequality parameters and noise coupling the fan out may be decreased. In this design, data latching is through four inverters to hold the internal node X. The delay of the circuit is obtained by the average value of the inverter's individual delay.

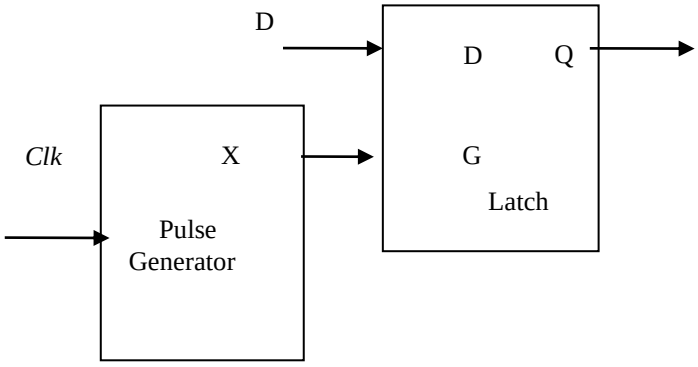

Fig: 1 Block Diagram of Pulse Triggered Flip-Flop

The main short come of this design is the pulse generator is turn on, on the rising edge of the clock at the node X. A pre-charging technique is also used to control the pre charge of in-house node.

II. Energy Metrics used for Flip-Flops design

III.1.*Power*

The power consumption of flip flop is categorising by the following type:
1. Consumption by the dynamic Power
2. Power consumption by short circuit
3. Power consumption by leakage

The entire power consumption is defined by the addition of all the powers that is defined by the following equation:

$$P = P_{dynamic} + P_{sc} + P_{leakage} \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

When the signal at CMOS circuit change their logic state from high to low or vice versa then dynamic Power expenditure occurs. Throughout this instance energy, the power is drained from the power supply to charges the output capacitance. This output capacitance causes the transition between 0V to V_{dd}[6,10]. The dynamic power consumption $P_{dynamic}$ is calculated as:

$$P_{dynamic} = \propto CV^2f \quad \ldots\ldots\ldots\ldots\ldots\ldots (2)$$

For a CMOS circuit both n type and p type transistor will turn on concurrently. When both the transistors are working at a same time the output of the circuit will be high. The PMOS is only working for falling edge of the transition to charge the output node capacitance. That power consumption is known as short circuit power consumption. That is also calculated by the following equation (3):

$$P_{sc} = I_{sc}V_{dd} \text{…………………………..} \quad (3)$$

Usually CMOS gate has non zero reverse leakage current and this current plays a vital role in the power dissipation even if the transistors are on sleep mode. The leakage power consumption is defined by the following equation:

$$P_{leakage} = I_{leakage}V_{dd} \text{…………………} \quad (4)$$

III.2. Propagation Delay

The propagation delay τ_p is the time taken by the logic circuit to produce the throughput [4]. This could be measured by the transition states of low to high τ_{PHL} and high to low τ_{PHL} signals.

τ_{PHL} and τ_{PHL} determine the input-to-output signal delay during the high-to-low and low-to-high transitions of the output respectively. By definition, τ_{PHL} is the delay between fifty percent transition voltage of rising input and 50% transition of falling output voltage. The average propagation delay is defined by the equation (5):

$$\tau_p = \frac{\tau_{PHL}+\tau_{PLH}}{2} \text{………………………………} \quad (5)$$

III.3. Power-Delay Product (PDP)

PDP is the total power consumption to produce the output in response of input. At the same time as the changes happens, the gate capacities can store up the energy. More rapidly the state changes, higher power will consume. Subsequently PDP be able to measure the transition properties of devices. Basically the following equation (6) can be defined PDP, where P is the average power dissipation.

$$PDP = P.\,\tau_p \text{………………………………………} \quad (6)$$

Also can be calculated by equation (7):

$$PDP = 2P_{avg}\tau_p \text{…………………………………} \quad (7)$$

Here, P_{avg} is average transition power dissipation at the maximum operating frequency.

III. Mathematical Behaviour of CDFF

The simulated diagram of proposed CDFF and the mathematical parameters are shown in the table II.

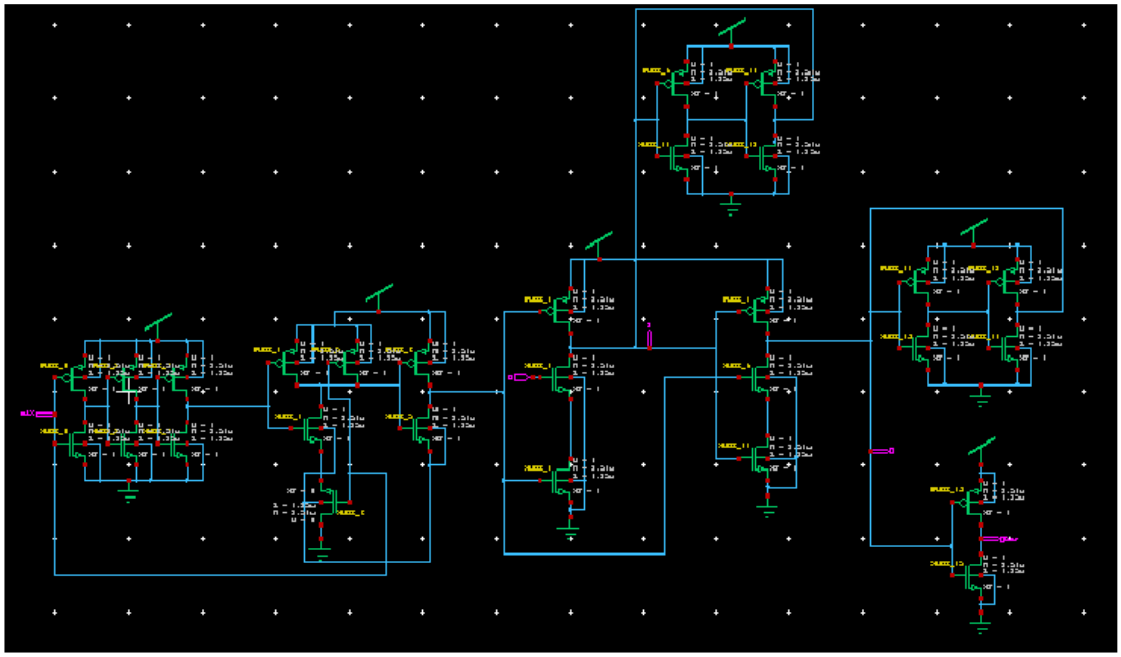

Fig: 2 Simulated Diagram of Explicit P-FF Design

TABLE II

S.No.	Parameter	Mathematical values
1	ε_{ox} (oxide permittivity)	3.5 x 10^{-13} F/cm
2	t_{ox} (oxide thickness)	$2.5 * 10^{-9}$
3	$V_{DS} = V_{Gs}$	1.8 V
4	c_{ox}	$1.4052 * 10^{-4}$
5	No. of transistor	28
For NMOS		
V_{Ton} (Threshold voltage) = 0.2607V		V_{Gs}=V_{DS}= 1.8V
W=500n and L=100n		I_D=$1.454 * 10^{-5}$A
K'= $2.527 * 10^{-6}$		μ_n = $1.799 * 10^{-2}$
For PMOS		
V_{Top} (Threshold voltage) = -0.303V		V_{Gs}=V_{DS}=1.8V
W = 400n and L = 100n		I_D=$6.694 * 10^{-8}$A
K'= $7.7286 * 10^{-9}$		μ_p = $5.50 * 10^{-5}$

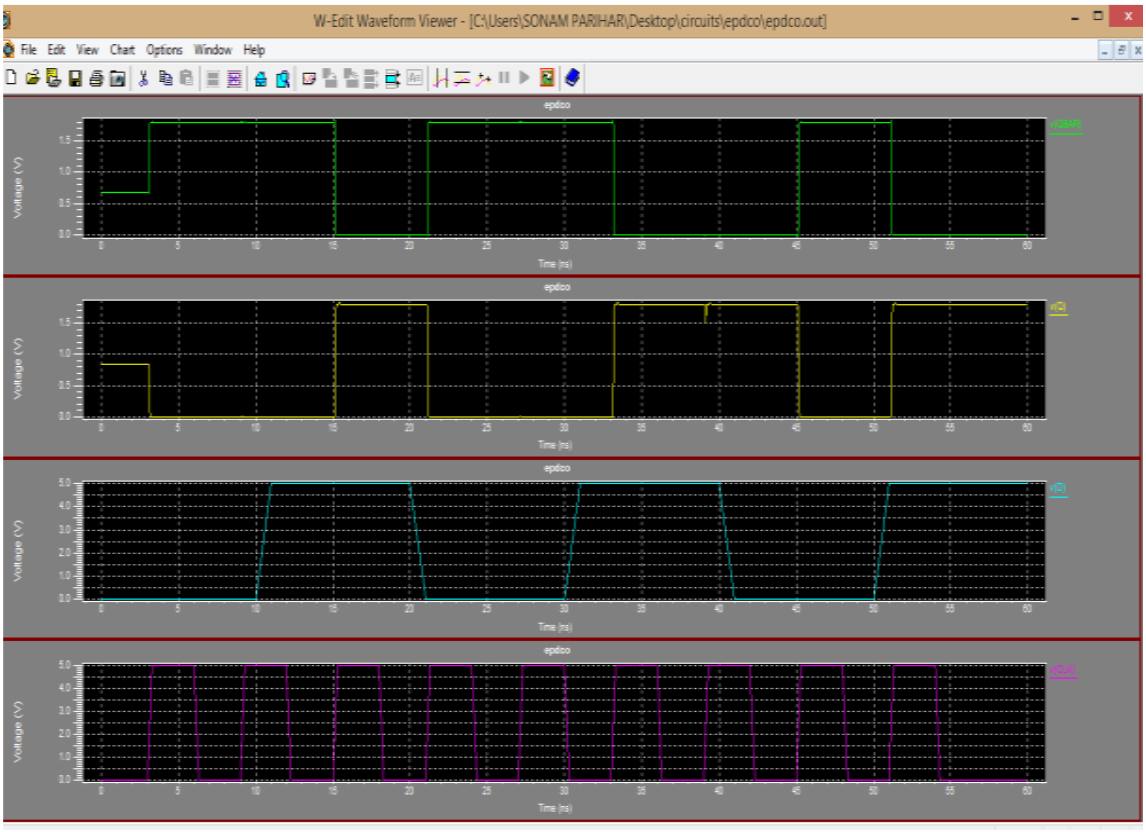

Fig: 3 Simulated waveform of Explicit P-FF Design

IV. Simulation Results

The proposed design has the different parameters obtained that are defined by the table-III. All the parameters are compared with conditional discharge flip-flop. By the conclusion table it is understandable that all the parameters are better than the previous one.

TABLE III

Flip flop	No of transistor	Propagation Delay at Q (n)	Propagation Delay o $\bar{Q}(n)$	Power Consumption	PDP of Q (n*f)	PDP of $\bar{Q}$
CDFF	30	22.511 nsec	13.514	12.37W	278.46	420.47
Proposed	28	11.247 nsecc	11.50 nsec	5.28W	59.384 16	58.470 6

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